

PG Certificate

in

VLSI Design & Verification

(RTL using Verilog, FPGA Design Flow & Verification)
(Live Project)

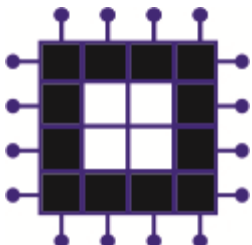
Certificates by
National Skill Development Corporation (NSDC),
Ministry of Skill Development &
Entrepreneurship (MSDE)

An Initiative by Industry Experts from Cadence,
Atrenta & Patni with qualification from IITs and
BITS-Pilani

Technology Partners of Cadence Design Systems,

Questa Vanguard Partner of Mentor Graphics,

HEP Partner of Mentor Graphics



DKOP Labs Pvt. Ltd.

Knowledge, Operations and Practices

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MODULE TOPICS

MODULE 1: VLSI DESIGN FLOW

1. VLSI design flow awareness

MODULE 2: LINUX OPERATING SYSTEM & SHELL SCRIPTING

1. Introduction to Linux OS
2. Commands for Managing files and directories
3. Methods of Securing Files in Linux
4. Document Processing commands
 - a) Filters
 - b) Redirection
 - c) Pipes
 - d) Wildcards
5. Creating files using the vi editor
6. vi Commands
7. Automating tasks using shell scripts
8. Using conditional execution in shell scripts
 - a) Arithmetic Conditions
 - b) String Conditions
 - c) File/Directory conditions
9. Managing repetitive tasks using shell scripts
 - a) Loops - While, Until, for
 - b) break and continue
10. Parameters Handling
11. Advanced features
 - a) functions
 - b) sed
 - c) awk
 - d) signal and traps

MODULE 3: DIGITAL SYSTEM IC DESIGN

1. Introduction to Digital System IC Design
2. Number System and Boolean logic
3. Logic gates, functions & library
4. Optimization techniques for logic functions
5. Designing combinational circuits
 - a) Error Detection and Correction Logic
 - b) Parity Generator and Checker
6. Analysis and Synthesis of combinational circuits
 - a) Arithmetic and Logical functions
 - b) Data Transmitters
 - c) Code Convertors
7. Logic Families
 - a) TTL
 - b) ECL
 - c) CMOS
8. Designing synchronous sequential circuits
9. Analysis and Synthesis of sequential circuits like Flip-Flops, registers, counters and memory
10. Basics of Microprocessor
11. Designing Finite State Machines (FSM)
12. Discussion - Special circuits like LFSR, FIFO, barrel shifter
13. Case study - UART

MODULE 4: VERILOG HDL

1. Introduction to Verilog HDL
2. Data types

3. Gate-Level modeling
4. Operators
5. Dataflow modeling
6. Modeling timing and delays
7. Behavioral modeling
8. Parameters, tasks and functions
9. Compiler directives
10. System tasks
11. File input/output
12. Switch-level modeling
13. User Defined Primitives
14. Design Case Studies - FSM, ALU, RAM, ROM, UART, Adaptive Traffic light signal

MODULE 5: PROJECT IN VERILOG

1. Project Study
2. Design & Implementation using Mentor Graphics ModelSim simulation tools
3. Evaluation of Project

MODULE 6: SYNTHESIS USING FPGA

1. Introduction to FPGAs and FPGA kits
2. Insight into FPGA Architecture
3. Writing RTL for FPGA flow
4. FPGA Design Flow using Xilinx FPGA Kit and Xilinx Tools
5. Using special FPGA Resources in design
 - a) Block RAM
 - b) DCM (Digital Clock Manager)
 - c) Dedicated arithmetic functions
6. FPGA kit interfacing and configuration
 - a) SSLED
 - b) PS2 Keyboard
 - c) VGA Controller
 - d) LCD Interfacing
 - e) A/D and D/A Converter Interfacing
 - f) Memory Module Interfacing

MODULE 7: TCL-TK

1. Introduction
2. Data types, variables, assignments and expressions
3. Lists, arrays and associative arrays
4. Subroutines or Procedures
5. Control structures
6. File Input and Output
7. The world of regular expressions
8. More on TCL - trace, eval, exec, info, history, format
9. Tk -frame, label, entry, check button, radio button, message box, scales, list box, scroll bar, text, menu, top level
10. Tk - binding, packing, grid, canvas
11. Tk - window manager commands, input focus, selection, update, grab, tkwait
12. Project in TCL-Tk

MODULE 8: VERIFICATION USING SYSTEMVERILOG

1. All about verification
2. Data types, operators
3. Procedural statements, tasks and Functions
4. Hierarchy and connectivity

5. Interfaces
6. Object oriented paradigm (OOPs)
7. Programs and clocking blocks
8. Inter-process communication
9. Randomization
10. System Verilog assertions
11. Functional coverage
12. Labs and project

MODULE 9: CMOS VLSI DESIGN

1. Introduction to CMOS design
2. MOS equations and characteristics
3. Basic CMOS concepts
4. Layout & Rules
5. Fabrication
6. Delay Estimations using logical effort
7. CMOS Combinational Circuits
8. CMOS Sequential Circuits
9. PSPICE simulation

MODULE 10: C/C++ REFRESHER

1. Basic Data Types
2. Operators (Arithmetic & Logical)
3. Conditional Constructs (if..else, switch..case, etc)
4. Repetition Constructs (loops)
5. Pointers
6. Object Oriented Programming
7. Classes and Objects
8. Inheritance & Polymorphism
9. Exercises

MODULE 11: PCB DESIGN

1. Schematic Capture
2. Creating SPICE Netlist
3. SPICE Simulation
4. Layout & Footprints
5. Gerber Generation

MODULE 12: SOFT SKILLS

1. Resume Writing
2. Interview Facing Skills
3. Mock Interview
4. Practice Tests

TOOLS

Our labs are equipped with Licenses of State-of-the-art Mentor Graphics EDA Tools, Windows/Linux based Open-Source EDA tools and demo versions of some industry tools.

1. Mentor Graphics Verilog Design & Simulation Tools
2. Open Source Verilog Design & Simulation Tool
3. Xilinx ISE for FPGA flow

BENEFITS FOR YOU

1. Helps you in understanding the **practical** and **industrial applications** of academic curriculum
2. Build your knowledge to develop **innovative projects** during your final year of engineering
3. Enhances the Skill-Set in your resume for **Better Placement Prospects** within the **Semiconductor Industry**
4. Helps the aspirants of **higher studies abroad** to face the stiff competition from students of other countries
5. Build your confidence through **hands on exposure** to various **tools & technologies**

TEAM OF TRAINERS

DKOP Labs is proud to have highly qualified and experienced professionals from Industry, Research and Academics. For details, [click here](#).

PLACEMENTS

We have been providing excellent placement platform to our trainees in companies like **Cadence, Xilinx, ST Microelectronics, Samsung, Synopsys, Mentor Graphics, SmartPlay, CMC Limited, TrueChip, Agnisys, DKOP Labs**, etc. For detailed list, [click here](#).

PARTNERSHIPS

TRAINING PARTNER OF NATIONAL SKILL DEVELOPMENT CORPORATION

HEP PARTNER OF MENTOR GRAPHICS

TECHNOLOGY PARTNER OF CADENCE DESIGN SYSTEMS

QUESTA VANGUARD PARTNER OF MENTOR GRAPHICS

PROGRAM DETAILS

Batch Commences in : January, March, July, Sept (every year)
Total Seats : 30 per batch (maximum)
Duration : Seven Months
(5 days/week, Mon-Fri, 4 hours/day)

This program is also available on Weekends (Sat & Sun) for working professionals.