PG Certificate
in
VLSI Design & Verification
(RTL using Verilog, FPGA Design Flow & Verification)
(Live Project)

(A Corporate Partner of IIT Delhi)


An Initiative by Industry Experts from Cadence, Atrenta & Patni with qualification from IITs and BITS-Pilani

DKOP Labs Pvt. Ltd.
Knowledge, Operations and Practices
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MODULE TOPICS

MODULE 1: VLSI DESIGN FLOW

1. VLSI design flow awareness

MODULE 2: LINUX OPERATING SYSTEM & SHELL SCRIPTING

1. Introduction to Linux OS
2. Managing files and directories
3. Securing Files in Linux
4. Managing documents
5. Creating files using the vi editor
6. Automating tasks using shell scripts
7. Using conditional execution in shell scripts
8. Managing repetitive tasks using shell scripts
9. Advanced features – functions, sed, awk, signal and traps

MODULE 3: TCL/TK

1. Introduction
2. Data types, variables, assignments and expressions
3. Lists, arrays and associative arrays
4. Subroutines or Procedures
5. Control structures
6. File Input and Output
7. The world of regular expressions
8. More on TCL - trace, eval, exec, info, history, format
9. Tk – frame, label, entry, check button, radio button, message box, scales, list box, scroll bar, text, menu, top level
10. Tk – binding, packing, grid, canvas
11. Tk – window manager commands, input focus, selection, update, grab, tkwait
12. Project in TCL-Tk

MODULE 4: ADVANCED DIGITAL DESIGN

1. Introduction to digital design
2. Number representation, complements and Boolean logic
3. Basic logic gates and logic functions
4. Optimization techniques for logic functions
5. Designing combinational circuits
6. Analysis of combinational circuits like, adders, comparator, multiplier etc.
7. Designing synchronous sequential circuits
8. Analysis of sequential circuits Flip-Flops, registers, counters, and simple processor
9. Designing Asynchronous Sequential Circuits
10. Designing Finite State Machines (FSM)
11. Discussion - Special circuits like LFSR, FIFO, barrel shifter etc.
12. Case study - UART

MODULE 5: VERILOG HDL

1. Introduction to Verilog HDL
2. Gate-Level modeling
3. Dataflow modeling
4. Operators
5. Data types
6. Modeling timing and delays
7. Behavioral modeling
8. Parameters, tasks and functions
9. Compiler directives
10. System tasks
11. File input/output
12. Switch-level modeling
13. User Defined Primitives

## MODULE 6: SYNTHESIS – FPGA DESIGN FLOW

1. Introduction to FPGAs and FPGA kits
2. Insight into FPGA Architecture
3. Writing RTL for FPGA flow
4. FPGA Design Flow using Xilinx FPGA Kit and Xilinx Tools
5. Using special FPGA Resources in design
   a. Block RAM
   b. DCM (Digital Clock Manager)
   c. Dedicated arithmetic functions
6. FPGA kit interfacing and configuration
   a. SSLED
   b. PS2 Keyboard

## MODULE 7: VERIFICATION USING SYSTEMVERILOG

1. All about verification
2. Data types, operators
3. Procedural statements, tasks and Functions
4. Hierarchy and connectivity
5. Interfaces
6. Object oriented paradigm (OOPs)
7. Programs and clocking blocks
8. Inter-process communication
9. Randomization
10. System Verilog assertions
11. Functional coverage
12. Labs and project

## MODULE 8: CMOS

1. Introduction to CMOS design
2. MOS equations and characteristics
3. Basic CMOS concepts
4. Layout & Rules
5. Fabrication
6. Delay Estimations using logical effort
7. CMOS Combinational Circuits
8. CMOS Sequential Circuits
9. PSPICE simulation
MODULE 9: PCB DESIGN & SPICE SIMULATION

1. PCB Design & Simulation Flow
2. Schematic Entry using OrCAD Capture
3. Basics of SPICE Netlist with concept of Models & Subcircuits
4. SPICE Simulation using OrCAD PSpice

MODULE 10: PROJECT WORK

1. Project Study
2. Design & Implementation using ModelSim simulator environment
3. Presentation
4. Document submission & Evaluation of Project

MODULE 11: SOFT SKILLS

1. Resume Writing
2. Interview Facing Skills
3. Presentation Preparation & Delivery
4. Aptitude & Company screening test preparation

PROGRAM DETAILS

Batches Commence on: Call for the dates

Total Seats : 30 per batch

Duration : Six Months
            (Four hours per day, 5 days/week, Mon-Fri)

Fees : Rs 67,416/- (60,000 + 12.36%) per student

Payment Terms:
• Rs 5,618/- (5000 + 12.36%) for registration
• Rs 33,708/- (30000 + 12.36%) on joining
• Rs 28,090/- (25000 + 12.36%) in 2\textsuperscript{nd} month
• Payment can be done by DD/Cheque in favor of “DKOP Labs Pvt Ltd” payable at Noida or can be deposited in cash/netbanking.

TOOLS

Our labs are equipped with State-of-the-art Mentor Graphics Tools, Windows/Linux based Open-Source EDA tools and demo versions of some industry tools.

• Verilog Design & Simulation Tools
• Open-Source SPICE Simulation Tools
• Xilinx ISE for FPGA flow
BENEFITS FOR THE STUDENTS

• Helps you in understanding the practical and industrial applications of academic curriculum

• Build your knowledge to develop innovative projects during their final year of engineering

• Enhances the Skill-Set in your resume for better placement prospects within the semiconductor industry

• Helping build knowledge and expertise for the aspirants of higher studies abroad to face the stiff competition from students of other countries

• Build your confidence through hands on exposure to various tools & technologies

DKOP TEAM

• Manu Lauria:
  
  
  o Experience:
    
    ▪ Around 5 years in Training Industry as Chairman of the Board at DKOP Labs Pvt Ltd. Have also been conducting training programs in Verilog, VHDL, SystemVerilog, TCL-Tk, Data Structures & Algorithms, etc.
    
    ▪ More than 18 years in the Semiconductor industry at Cadence Design Systems, being responsible for many products from concept to reality. Was part of the core leadership team of Cadence’s Noida Center for 13 years. Has managed or been part of teams that developed products in the areas of Synthesis, Simulation, Custom IC Design, Rule checking, Model Development & Web based component/design management.
    
    ▪ Around 4 years at ONGC.

• Devender Khari:
  
  o Qualification: M.E. Computer Science from BITS, Pilani and B.Tech in Computer Engineering from Shivaji University.
Experience:

- More than 6 years in Training Industry as CEO of DKOP Labs Pvt Ltd. Have also been conducting training programs in Linux Shell Scripting, Data Structures & Algorithms in C, PCB Design using OrCAD, Android, Responsive Web Development, PHP, JAVA, J2ME, etc.

- More than 8 years in Cadence Design Systems. Have worked in the R&D of OrCAD suite of tools, Allegro Design Editor and Virtuoso Composer.

- Around a year and a half with Bunka Orient India (GrapeCity).

- Expert in developing Software for Engineering applications as well as Web Technology and Mobile based applications. Proficient in C, C++, PHP and JAVA.

- Chandrakant Sakharwade:
  

  - Experience:

    - Around three years in Training Industry as Director at DKOP Labs Pvt Ltd. Have been involved in conducting training programs in PCB Design, Embedded Systems, Digital Electronics, etc.


- Ajay Sharma:
  
  - Qualification: M.Sc. In Electronic Science from Electronic Science Department, Kurukshetra University (2003)

  - Experience:

    - Around three years in Training Industry as Manager, VLSI Design Division at DKOP Labs Pvt Ltd. Have been conducting training programs in Digital Electronics, Verilog, FPGA and CMOS, etc. Have also worked on many research projects in VLSI Design domain.
- 6+ years of Research Experience in the field of **ASIC Design**. Spent 3 years in research on **Smart Sensor ASICs** at **SRL, University of Warwick, UK**. Contributed in the whole flow from Circuit Design to Tapeout. Handled MIT (Ministry of Information Technology) initiative project, SMDP-II, at **NIT, Jalandhar** for year and a half. Played an instrumental role in taking designs from Circuit to Layout. Guided Masters and Bachelors Projects.

- **Neeraj Aggarwal:**
  - **Qualification:** *M.Tech.* in CS from **Jawahar Lal Nehru University (JNU), Delhi**
  - **Experience:**
    - More than 6 months in Training Industry as **Consultant** at **DKOP Labs Pvt Ltd**. Have been involved in conducting training programs in **Telecom domain**.
    - More than 21 years of experience in Telecom industry in Aricent, Verizon & TCS. Proven ability in Business analysis, Project planning & Execution, Functional designing, Learning and Development in Communication domain. High achiever who loves using innovation to solve challenges. Worked very closely with the numerous customers to achieve their business goals. Certified TMF Telecom consultant with expertise in process improvement.

- **Nitin Tiwari:**
  - **Qualification:** *M.Tech.* in VLSI Design, **VIT University**
  - **Experience:**
    - More than 2 years of experience in SMDP Program at **NIT, Jalandhar**
    - Responsible for the Design projects executed under SMDP initiative and maintenance of CAD tools of Cadence, Synopsys and Mentor Graphics.

- **Jyotika Taneja:**
  - **Qualification:** *M.Tech.* in VLSI Design from **Banasthali University, Rajasthan**
  - **Experience:**
    - Started his career at DKOP Labs as a VLSI Design Engineer in May 2013. Handling multiple projects and training programs in VLSI Design.
Companies where we have placed our students

**XILINX, HYDERABAD**
- Sahil Goyal, Lovely Professional University
- Vishal Mahajan, Sri Sai College of Engg & Tech, Badhani, Punjab

**SAMSUNG, NOIDA**
- Kunal Sharma, Ambedkar Institute of Technology, New Delhi
- Sagar Joshi, Ambedkar Institute of Technology, New Delhi
- Vinit Saddyan, MMEC, Mulana

**ST MICROELECTRONICS, GREATER NOIDA**
- Kavita Sharma, Banasthali University

**CADENCE DESIGN SYSTEMS, NOIDA**
- Sorabh Dung, LIT, Lovely Professional University
- Ruchi Mittal, CDAC
- Rameet Pasricha, JIIT, Noida
- Rachna Raj, Banasthali University
- Saloni Maheshwari, Banasthali University
- Sachin Kumar, LIT, Lovely Professional University
- Jupinder Kaur, LIT, Lovely Professional University
- Manvi Goel, Banasthali University
- Balveer Singh Koranga, GB Pant Engineering College, Pauri, Uttarakhand
- Dilpreet Singh, Lovely Professional University
- Mayank Pandey, ITS Engg College, Greater Noida
- Utkarsh Kumar, Lovely Professional University
- Aparna Upreti, Banasthali University
- Shailey Chaudhary, Banasthali University
- Priyanka Jain, Banasthali University
- Balpreet Kaur, Lovely Professional University, Jalandhar
- Animesh Tanwar, ITM, Gurgaon
- Rakesh Gupta, BMIT, Sonipat
- Jatin Garg, MMEC, Mulana
- Manuj Gupta, BKBIE, Pilani
- Saksham Nayar, ITM, Gurgaon
- Kashish Kaul, ITM, Gurgaon
- Vivek Negi, UIT, Dehradun
- Shruti Kejriwal, Mody Institute of Technology & Science, Lakshmangarh, Rajasthan
- Rajat Verma, MMEC, Mulana

**MENTOR GRAPHICS, NOIDA**
- Vikas Tomar, ITM, Gurgaon
- Jitendra Aggarwal, Amity University, Noida
- Sonam, DCR Univ Sc Tech, Murthal
- Sweety Gupta, Maharja Agarsen Institute of Technology, Delhi
- Sunil Bansal, DCR Univ, Murthal
SYNOPSYS, DELHI
Nidhi Gupta, M.P.C.T., Gwalior
Prishkrit Abrol, DAVIET, Jalandhar
Pankaj Talwar, LCET, Ludhiana
Richa, Banasthali University
Mamta Rana, Jiwaji University

SYNOPSYS, BANGALORE
Pawan Srivastava, GNIT, Greater Noida

SYNOPSYS, NOIDA
Jayant Gautam, North Maharashtra University, Maharashtra
Siddharth Deshwal, ITS, Greater Noida

AGNISYS, NOIDA
Sandeep Thakur, Lovely Professional University
Amit Kapoor, SSIEET, Dera Bassi
Nitin Ahuja, BSAITM, Faridabad
Rohit Singh Bhadana, BSAITM, Faridabad
Vipin Kumar, Maharaja Agarsen Institute of Technology, Delhi
Rinku Singh, BBDIT, Ghaziabad
Munish Kumar, Swami Sarvanand Giri Panjab Univ. Regional Center, Hoshiarpur
Kiran Sharma, Banasthali University
Sudhanshu Tripathi, GNIT, Greater Noida
Meenakshi Bisht, Rayat Bahra, Ropar

TRUECHIP, NOIDA
Abhishek Goel, MMEC, Mulana
Nitin Verma, Maharaja Agarsen Institute of Technology, Delhi

MASAMB, NOIDA
Rishabh, Maharaja Agarsen Institute of Technology, Delhi
Pawan, Maharaja Agarsen Institute of Technology, Delhi
Heetashi Arora, ITM – Gurgaon
Varun Sharma, JIIT – Noida
Abhinav Panwar, Gurukul Kangri University- Hardwar

CMC, HYDERABAD
Savita Garg, Banasthali University
Nidhi Bhardwaj, GTBIT, Delhi
Saurabh Kumar, Uttarakhand Technical University, Dehradun
Vaibhav Singh, MDU, Rohtak

CIRCUITSUTRA TECHNOLOGIES, NOIDA
Parvinder Pal Singh, Lovely Professional University
Navya Prabhakar, GTBIT, GGSIP University, Delhi

DKOP LABS, NOIDA
Rahul Kumar, Rai University
Pushpinder Singh, SVIET – Banud
Amitav Banerjee, UPTU
Ravi Bhardwaj, Lovely Professional University
Jyotika Taneja, Banasthali University

PERFECT VIPS, BANGALORE
Himanshu Dixit, GNIT, Greater Noida
Aditi Saini, Banasthali University

TRIDENT TECH LABS, DELHI
Bhanu Pratap, Lovely Institute of Technology, Jalandhar

RF SILICON, NOIDA
Nirmal Singh, UPTU

HP, BANGALORE
Hariom Pandey, UPTU

SASKEN, BANGALORE
Sumit Gupta, Thapar - Patiala
Sumit Kumar, Thapar - Patiala

PHOENIX, NOIDA
Akhilesh Singh, Jiwaji University

OM NANOTECHNOLOGY, GREATER NOIDA
Mohammed Sharique, Jiwaji University

UNIVERSITIES IN USA, CANADA & GERMANY
Smriti Gurung
Subeg Singh
Binipal Wadhwa
Hasan Karkara
Vidushi Bansal
Rahul Yadav

DKOP PARTNERSHIPS

TECHNOLOGY PARTNER OF CADENCE DESIGN SYSTEMS

QUESTA VANGUARD PARTNER OF CADENCE DESIGN SYSTEMS

CORPORATE PARTNER OF IIT, DELHI

KNOWLEDGE PARTNERS OF THE FOLLOWING INSTITUTES AND UNIVERSITIES
• NIT, Jalandhar
• Galgotia College of Engineering & Technology, Greater Noida
• Maharaja Surajmal Institute of Technology, Delhi
• Sharda Group of Institutions, Agra
• Greater Noida Institute of Technology, Greater Noida
• Lovely Professional University, Phagwara
• Echelon Institute of Technology, Faridabad
• SRM University, Chennai
• St Margaret Engineering College, Neemrana
• Maharaja Agarsen College, Delhi University
• UIET, Kurukshetra University